DC–40 GHz and 20–40 GHz MMIC SPDT Switches

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Abstract—**DC to 40 GHz and 20 to 40 GHz monolithic GaAs SPDT switches have been demonstrated. Both the measured and the modeled small-signal performance are presented. Measured power handling performance and switching speed data are also presented. The 20–40 GHz switch uses a combination of shunt FET's and quarter-wave transformers. Better than 2 dB insertion loss and 25 dB isolation have been achieved. The dc–40 GHZ switch uses a combination of series and shunt FET's. Better than 3 dB insertion loss and 23 dB isolation have been achieved. A simplified switching FET model is used to adequately model switch performance. It is demonstrated that parasitic "off" state resistance is an important FET characteristic for broad-band switch design. The switches use MESFET's with the same characteristics as an existing millimeter-wave amplifier to allow for ease of future integration.**

I. INTRODUCTION

THIS PAPER discusses A 20–40 GHz SPDT switch composed of shunt FET switching elements and quarter-wave transformers, and a dc–40 GHz SPDT switch composed of series and shunt FET switching elements. These switches are similar in topology to MMIC switches previously demonstrated at lower frequencies.

A bandwidth greater than one octave (6–19 GHz) has been demonstrated using shunt FET's as switching elements in conjunction with quarter-wave transformers [1]. The present work includes a similar design to cover the 20–40 GHz band.

Various configurations have been described using combinations of series and shunt switching elements for broad-band applications [2]–[4]. The dc–40 GHz MMIC SPDT switch described in this paper incorporates series and shunt FET switching elements. The topology of this switch allows operation over extremely large bandwidths. The series FET allows the switch to operate down to dc.

Switching quality factor is used as a figure of merit for switching devices. Two switching quality factors are commonly used—the simple switching quality factor (Q_s) and the Kurokawa and Schlosser quality factor ($\hat{Q}$) [5]. Q_s is the ratio of the magnitude of the device impedance in the "off" state to the magnitude of the device impedance in the "on" state. $\hat{Q}$ is given by

$$\hat{Q} = \frac{\sqrt{(R_1 - R_2)^2 + (X_1 - X_2)^2}}{\sqrt{R_1 R_2}}$$

where $R_1 + jX_1$ and $R_2 + jX_2$ are the device impedances in the two states.

Standard millimeter-wave MMIC amplifier FET's have been used in the dc–40 GHz and 20–40 GHz switches to allow the switches to be integrated with other millimeter-wave circuitry in the future. These FET's have a low switching quality factor. Q_s is less than 5 at 40 GHz, and $\hat{Q}$ is less than 10 at 40 GHz. Although low switching Q's do indicate general limits in switch performance, they do not accurately predict switch performance for the circuit configurations described in this paper. The parasitic resistance in the "off" state is an important switch FET characteristic, but its effect is not accounted for in Q_s. The switch designs in this paper incorporate "off" state capacitance in an artificial transmission line. Neither Q_s nor $\hat{Q}$ accurately predicts switch performance for a device in such a configuration.

II. SWITCH FET MODEL

The use of FET's as switching elements is well documented [6], [7]. In switching operation, a drain bias is not applied. The bidirectional RF signal path is between the source and the drain. The configuration of a switching FET is indicated in Fig. 1(a). In the "on" state the gate is biased at 0 V. The "on" state can be adequately modeled by the dc "on" resistance between the source and the drain (R_{on}), as is shown in Fig. 1(b). Additional parasitic elements are present, but have no significant RF effect, particularly if the gate bias circuitry is isolated with a large value resistor, as is indicated in Fig. 1(a). In the "off" state the gate is biased beyond pinch-off. A complete equivalent circuit in the "off" state is shown in Fig. 1(b). This equivalent circuit is based on device geometry and has been described previously [6], [7]. The "off" state source-to-drain leakage resistance (R_{ds}) is generally large enough to be neglected in circuit modeling. The source and the drain are capacitively coupled directly (C_{sd}) and also through the gate (C_{gs} and C_{gd}). All of these capacitances have series parasitic resistive elements (R_{gs} and R_{gd} for C_{gs} and C_{gd}; R_s and R_d for C_{sd}). Although the elements of the FET equivalent circuit model in Fig. 1(b) are relatively straightforward to calculate [6], [7], measurement of the individual elements is impractical. Not only is it difficult to confirm the details of this equivalent circuit by measurement, such a detailed equivalent circuit is unnecessary for accurate circuit modeling. A simplified FET model

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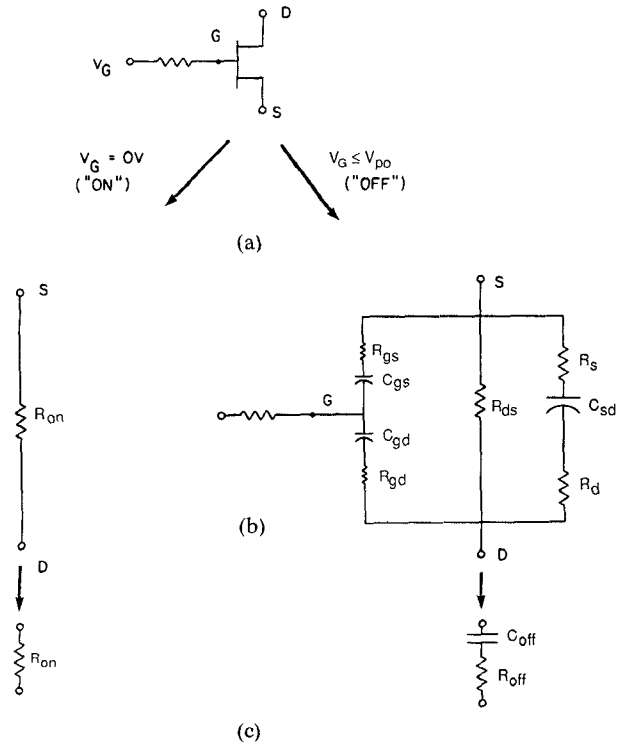

Fig. 1. (a) FET in switching configuration. (b) Complete equivalent circuit. (c) Simplified equivalent circuit.

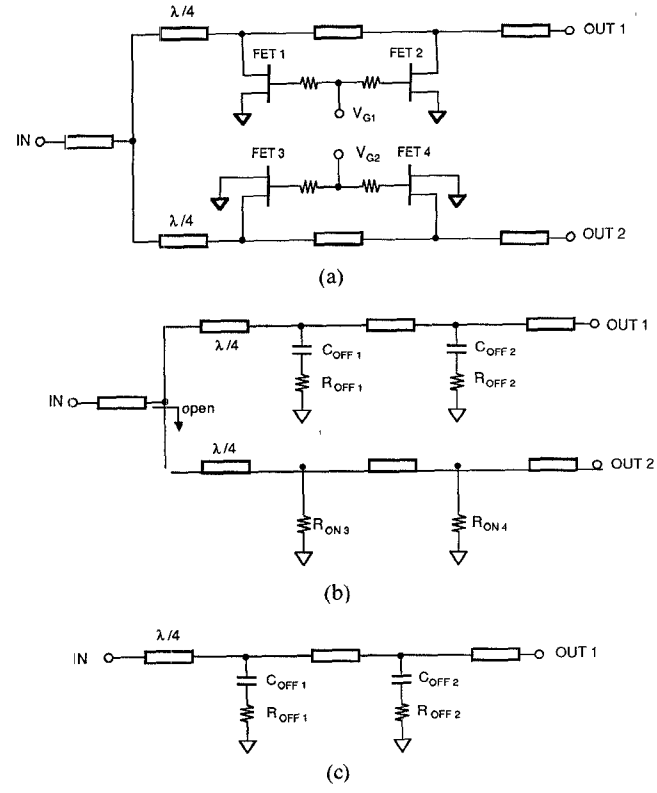

Fig. 2. (a) Topology of the 20–40 GHz SPDT switch. (b) Equivalent circuit when switched to OUT1. (c) Artificial transmission line approximation.

can be used without sacrificing accuracy, and its values are readily measured.

A simplified FET model is indicated in Fig. 1(c). The "on" state equivalent circuit is unchanged. The "off" state equivalent circuit has been reduced to a simple series resistor and capacitor. Since R_{ds} is typically very large, it has been neglected. It is straightforward to include R_{ds} if needed. R_{off} and C_{off} can be calculated from the resistive and capacitive elements in Fig. 1(b). The calculation is simplified if it is assumed that the magnitudes of the various capacitive reactances are much larger than the various parasitic resistances. This is true up to 40 GHz for the devices used in the dc–40 GHz and 20–40 GHz switches reported in this paper. This assumption yields the following relationships:

$$R_{\text{off}} \approx \frac{R_{gs}+R_{gd}}{\left[1+\dfrac{C_{sd}}{(C_{gs}+C_{gd})}\right]^2} + \frac{R_s+R_d}{\left[1+\dfrac{(C_{gs}+C_{gd})}{C_{sd}}\right]^2}$$

$$1/C_{\text{off}} \approx \frac{1/(C_{gs}+C_{gd})}{\left[1+\dfrac{C_{sd}}{(C_{gs}+C_{gd})}\right]^2} + \frac{1/C_{sd}}{\left[1+\dfrac{(C_{gd}+C_{dg})}{C_{sd}}\right]^2}.$$

Note that these relationships for R_{off} and C_{off} are frequency independent. The additional terms that have been ignored are frequency dependent.

The value of C_{off} can readily be determined by RF measurements. The value of R_{off} is more difficult to measure. The insertion losses of the dc–40 GHz and 20–40 GHz switches presented in this paper are sensitive to R_{off} at frequencies approaching 40 GHz. Thus the dc–40 GHz and 20–40 GHz switches are suitable vehicles for determining the value of R_{off}.

III. Circuit Design and Modeling

The topology of the 20–40 GHz SPDT switch is indicated in Fig. 2(a). For clarity, the schematic is labeled with an input (IN) and two outputs (OUT1 and OUT2). Since the switch is bidirectional, the input and outputs can be reversed. In this circuit the switching FET's are used in a shunt configuration in conjunction with quarter-wavelength transformers. The circuit is composed of two equal and independently biased arms. Fig. 2(b) shows normal operation with the switch biased to pass signals between IN and OUT1. The FET's are represented as their simplified equivalent circuits. The FET's in the OUT1 arm (FET1 and FET2) are pinched off, and act primarily as shunt capacitances. The FET's in the OUT2 arm (FET3 and FET4) are biased in the "on" state and act as shunt resistances. FET3 and FET4 present a low impedance to the quarter-wavelength transformer. The quarter-wavelength transformer is used to transform the low impedance into a high impedance. Such transformers can be effective over bandwidths of an octave or more.

Fig. 2(c) indicates a further simplification, in which only the effects of the OUT1 arm are included. In circuit modeling, the effect of the OUT2 arm is not neglected since it is a significant contributor to insertion loss. By looking at the

OUT1 arm alone (as in Fig. 2(c)), other loss mechanisms can be more clearly illustrated. All the transmission lines are inductive (characteristic impedance is greater than 50 Ω), thus Fig. 2(c) shows that this arm of the switch can be approximated as an artificial transmission line. The major cause of loss in such an artificial transmission line is the parasitic resistance for each shunt capacitor (R_{off}). This is analogous to the gate line in a distributed amplifier where an artificial transmission line is realized by the gate capacitance and series inductors [8]. The parasitic gate resistance in such a gate line is the primary cause of gate line attenuation. Thus it can be seen that R_{off} is an important contributor to the insertion loss of this switch and should not be neglected.

The artificial transmission line representation not only reveals the losses due to R_{off}, it also gives insight into how satisfactory switch performance can be achieved with devices having a low switching quality factor. In the switch in Fig. 2, the "off" state capacitance (C_{off}) is incorporated into the artificial transmission line and does not directly contribute to insertion loss. C_{off} couples power into R_{off}, and thus affects the attenuation due to R_{off}. When biased in the opposite state, R_{on} attenuates the signal, and provides isolation. Because C_{off} is incorporated into an artificial transmission line, very low values of Q_s or $\hat{Q}$ can be tolerated. It is possible to construct a useful switch using FET's with a very low Q_s or $\hat{Q}$.

The dc–40 GHz SPDT switch has the topology shown in Fig. 3. Series FET's (FET1 and FET4) are used in place of the quarter-wavelength transformers from Fig. 2. The series FET in the OUT1 arm (FET1) is biased together with the shunt FET's in the OUT2 arm (FET5 and FET6). Fig. 3(b) shows the switch when biased to pass signals between IN and OUT1 with the FET's represented by equivalent circuits. In this state the OUT2 arm consists of C_{off4} and R_{off4} from FET4 followed by shunt resistances R_{on5}, R_{on6}, and the 50-Ω termination. The circuit model may be simplified to Fig. 3(c) if the resistive elements in the OUT2 arm are lumped together as R_2, where R_2 at dc is

$$R_2 = R_{off4} + R_{on5} \| R_{on6} \| 50\Omega.$$

This relationship is only true at dc, but is approximately correct up to 40 GHz for the switch presented in this paper. Note that the major component of R_2 is R_{off4}. The simplified circuit model in Fig. 3(c) is essentially an artificial transmission line, with an additional series resistance (R_{on1}). R_{on1} causes a loss which is essentially constant over frequency. It is the dominant component of dc insertion loss. The artificial transmission line approximation illustrates how the shunt parasitic resistances (R_2, R_{off2}, and R_{off3}) cause the insertion loss to increase with frequency. This confirms the importance of R_{off} in broadband switch performance.

IV. MMIC Fabrication

The dc–40 GHz and 20–40 GHz switch circuits have been fabricated as GaAs MMIC's. An active layer doping of 3×10^{17} cm^{-3} and a contact layer doping of 1×10^{18} cm^{-3} were realized with two Si implants: 2.0×10^{13} cm^{-2} at 60 keV and 9.1×10^{12} cm^{-2} at 400 keV (assuming 100 percent activation). The FET channels were etched for an I_{dss} of 170 mA/mm, yielding a pinch-off voltage of −1.4 V. The 0.35-μm gates were E-beam defined. Polyimide passivation was used over active FET regions and under air bridges. The gates are biased through 1.5 kΩ open gate FET resistors. No other resistor types and no capacitors were used. Transmission lines are realized with 3-μm-thick plated gold with a minimum line width of 10 μm. The substrate was thinned to 100 μm, 50-μm square via holes were dry etched, and the backside was plated with gold.

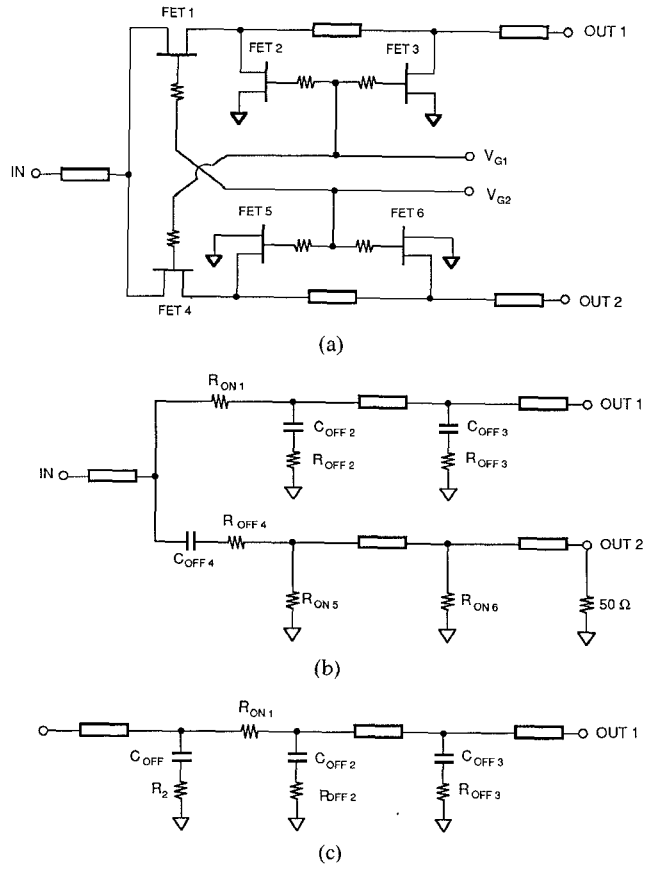

Fig. 3. (a) Topology of the dc–40 GHz SPDT switch (b) Equivalent circuit when switched to OUT1. (c) Artificial transmission line approximation.

The completed dc–40 GHz switch is shown in Fig. 4. It has a total gate periphery of 430 μm (not including bias resistors). The series FET's have two gate fingers and an air-bridged source. The shunt FET's each have a single gate finger. This allows the shunt FET's to be made without air bridges and reduces inductance to ground. The completed 20–40 GHz switch is shown in Fig. 5. It has a total gate periphery of 560 μm (not including bias resistors). Two of the shunt FET's have two gate fingers and an air-bridged source; the other two have a single gate finger. Both switches are fully self-contained MMIC's, with no external bias circuitry required. The dc–40 GHz switch is 33×50 mils (0.84×1.27 mm). The 20–40 GHz switch is 50×50 mils (1.27×1.27 mm).

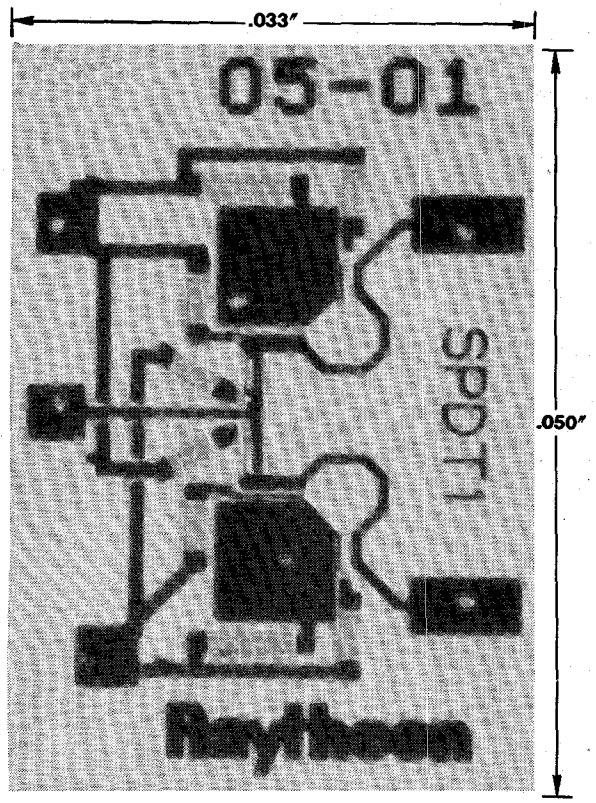

Fig. 4. Photograph of the dc–40 GHz SPDT switch.

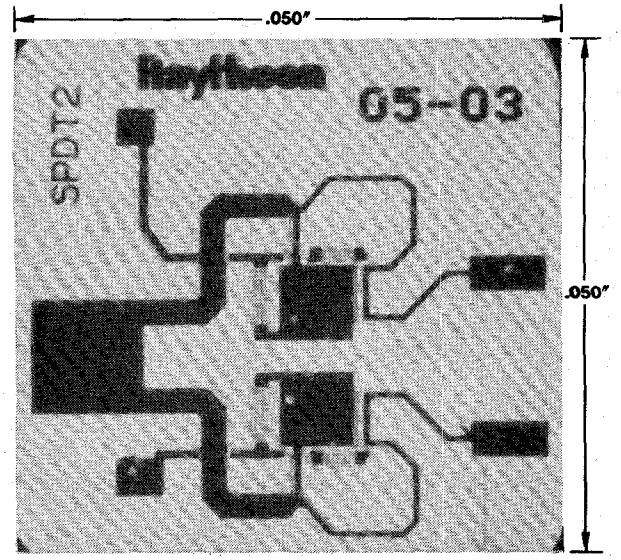

Fig. 5. Photograph of the 20–40 GHz SPDT switch.

V. Measured and Modeled Performance

The measured and modeled small-signal performance of the dc–40 GHz switch is shown in Fig. 6. The measured insertion loss is between 2 dB and 3 dB from dc to 40 GHz. Isolation is in excess of 25 dB from dc to 20 GHz, and gradually degrades to 23 dB at 40 GHz. Test fixture loss was removed from the insertion loss and isolation measurements, but the effect of the test fixture has not been removed from the return loss measurements. The test

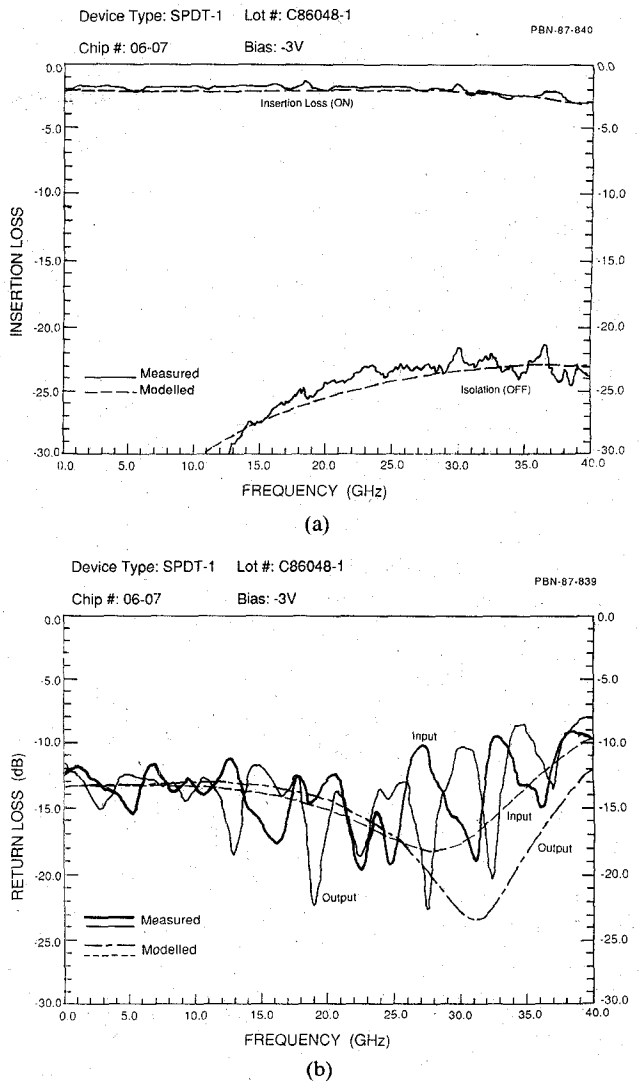

Fig. 6. Measured and modeled performance of the dc–40 GHz SPDT switch. (a) Insertion loss and isolation. (b) Return loss.

fixture itself has a maximum insertion loss of 1 dB (at 32 GHz) and return loss peaks of up to 13 dB (above 25 GHz). Return loss is 10 dB or better over the dc–40 GHz band with the exception of a single peak of 9 dB at 35 GHz. The modeled performance of the switch is included in Fig. 6. The model uses the dc measured values of R_{on} (R_{on} varies between 2.7 Ω·mm and 3 Ω·mm). C_{off} was measured to be 0.3 pf/mm on test devices, and this value is used in the models. A value of 0.7 Ω·mm was used for R_{off}. Microstrip discontinuities and transitions were modeled [9], [10]. Via hole inductance (25 pH) was also included. This relatively simple circuit model provides very good agreement with measured results. The poorest agreement is in the return losses (Fig. 6(b)), but the measurement includes considerable test fixture effect which is not included in the model.

The measured and the modeled performance of the 20–40 GHz SPDT switch are shown in Fig. 7. From 18 to 40 GHz the insertion loss is less than 2 dB. The isolation is 25 dB over most of the band, degrading to 23 dB at the low band edge. Test fixture loss was removed from the

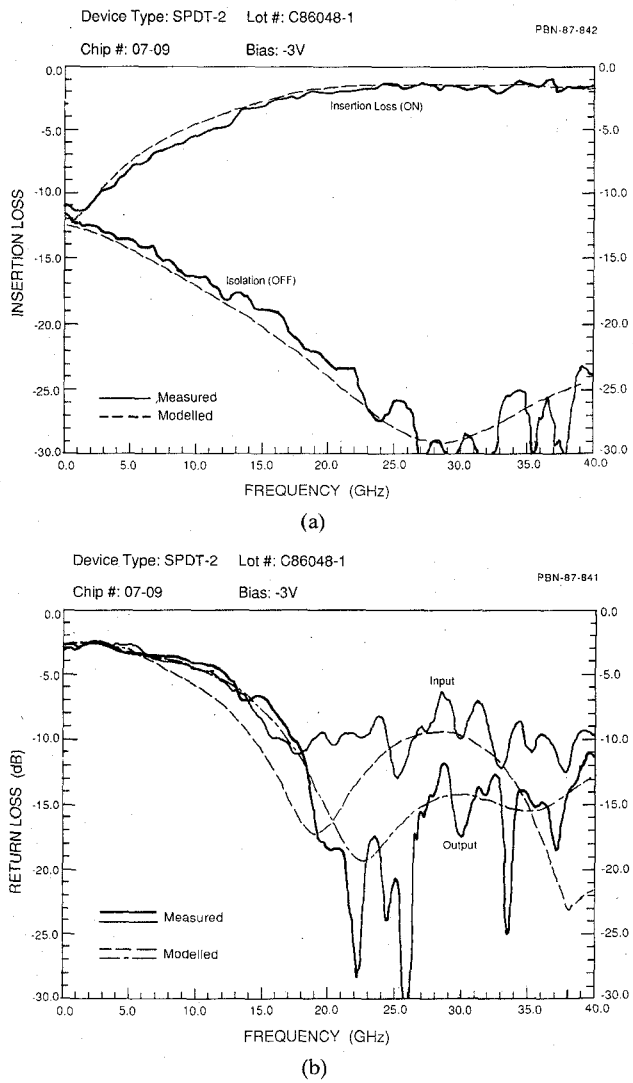

Fig. 7. Measured and modeled performance of the 20–40 GHz SPDT switch. (a) Insertion loss. (b) Return loss.

insertion loss and isolation measurements, but no attempt was made to remove the effects of the test fixture from the return loss measurements. The characteristics of the test fixture are the same as for the dc–40 GHz switch. The return loss at the input is better than 10 dB over the band. The output return loss averages 10 dB over the band, but has occasional peaks up to 7 dB. The modeled performance for the switch is included in Fig. 7. This switch was modeled using the same models and parameters as the dc–40 GHz switch. For this switch the measured value of R_{on} was 3 $\Omega \cdot$mm for all the FET's. The agreement between the measured and the modeled performance is very good. The poorest agreement is for the return loss measurements, which include considerable test fixture contributions.

The switch models can be used to determine the contribution R_{off} makes to insertion loss. The dc–40 GHz switch has a maximum insertion loss of 3 dB. Of this loss, 1 dB is due to R_{off} (the remainder of the loss is primarily due to the series FET's). The 20–40 GHz switch has an insertion loss of 2 dB at 40 GHz. Of this loss, 1 dB is due to R_{off} (the remainder is due to the other switch arm not

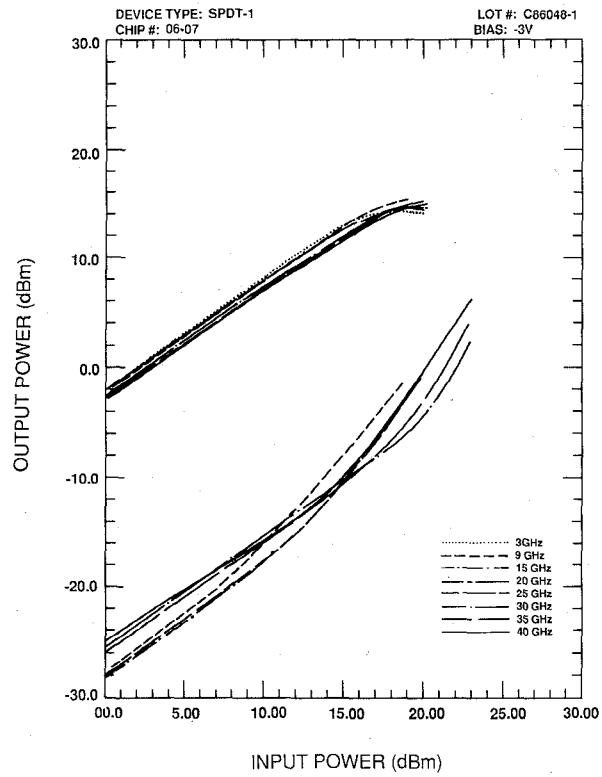

Fig. 8. Insertion loss and isolation for the dc–40 GHz SPDT switch over power.

providing an ideal open circuit through the quarter-wave transformer). Clearly the effect of R_{off} is significant and should not be neglected.

Insertion loss and isolation have also been measured at power levels up to 25 dBm (300 mW). Fig. 8 shows insertion loss and isolation transfer curves for the dc–40 GHz switch at various frequencies across the band. Insertion loss increases by 1 dB at 18 dBm (60 mW). This effect is caused by current limiting in the series FET's. The isolation degrades more gradually. Isolation is still better than 20 dB at 20 dBm (100 mW) at all frequencies. Note the isolation is not shown at 3 GHz. At low frequencies, the isolation was too high to measure accurately. At 3 GHz the isolation was much better than 20 dB at 20 dBm. The degradation in isolation is caused by current limiting in the shunt FET's.

Fig. 9 shows the power transfer curves for insertion loss and isolation for the 20–40 GHz switch. Insertion loss is not significantly degraded until 23 dBm (200 mW). Since there are no series FET's, insertion loss degradation is due to voltage swing across the shunt FET's. Isolation degrades significantly for power levels about 15 to 20 dBm (30 to 100 mW) depending on frequency. Isolation degrades because of current limiting in the shunt FET's. Current limiting degrades isolation well before voltage limiting degrades insertion loss.

For both of these switches the dominant cause of power limiting is current limiting through the FET's. The I_{dss} for the FET's in these switches averages 170 mA/mm. It would be possible to double the current of the FET's by

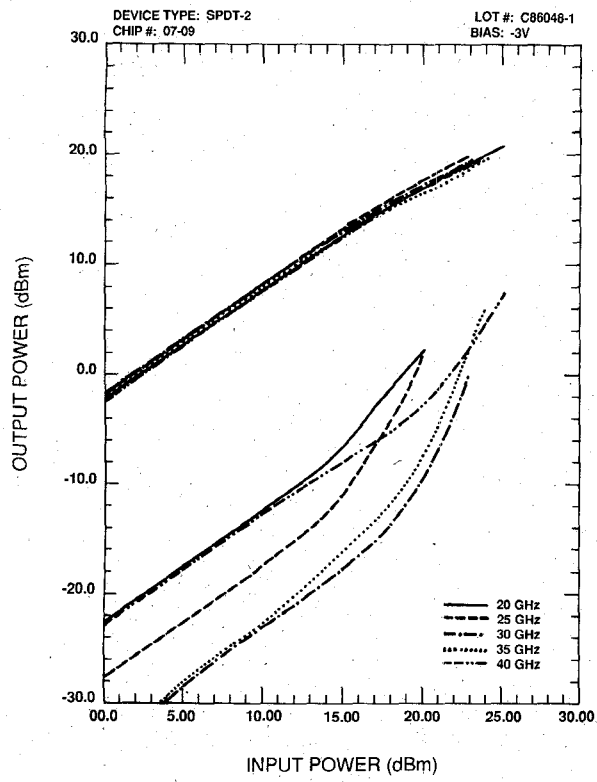

Fig. 9. Insertion loss and isolation for the 20–40 GHz SPDT switch over power.

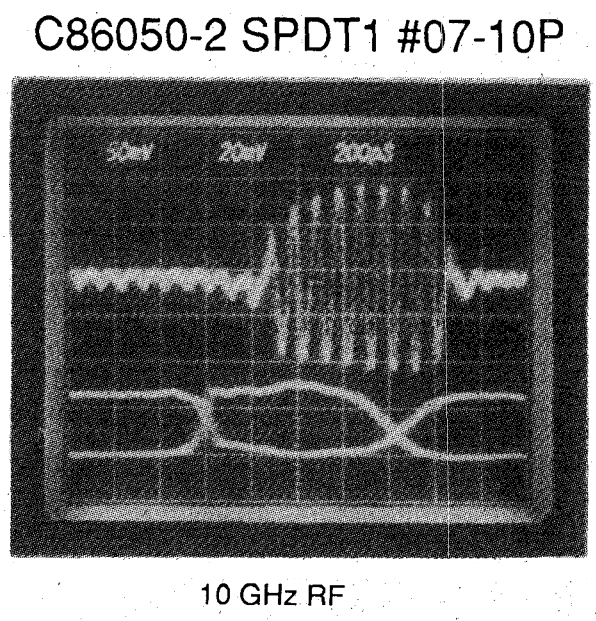

Fig. 10. Switching speed for the dc–40 GHz SPDT switch.

increasing the channel thickness. The pinch-off voltage of the resulting devices would be approximately −3 V. This would not have a large effect on small-signal performance. R_{on} and C_{off} have been shown to decrease [11], and R_{off} is also expected to decrease with such a change in pinch-off voltage, providing a small improvement in small-signal performance. Power handling would increase by as much as 6 dB, or until the voltage limit was reached. These

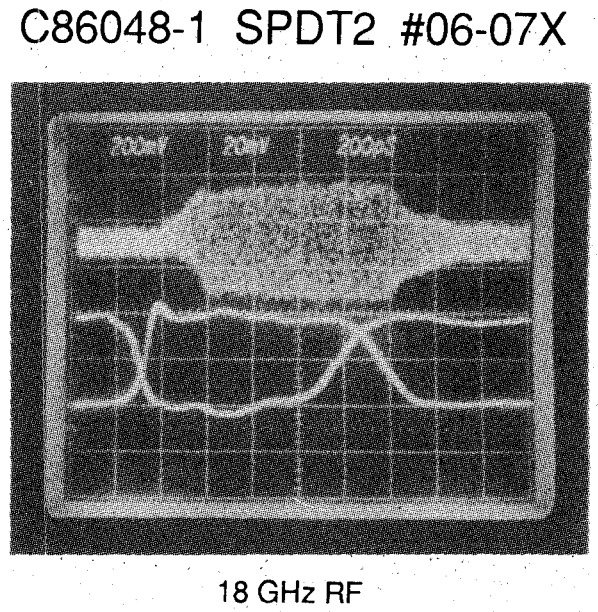

Fig. 11. Switching speed for the 20–40 GHz SPDT switch.

FET's would no longer be similar to the existing millimeter-wave amplifier FET's, and commonality would be sacrificed.

Switching speed has been measured for both switches. Fig. 10 shows the detected 10-GHz RF output from the dc–40 GHz switch in the top trace and the complementary bias inputs in the bottom trace. The turn-on time is less than 400 ps; the turn-off time is less than 300 ps. Fig. 11 shows the switching speed for the 20–40 GHz switch with an 18-GHz RF. The turn-on time is less than 300 ps and the turn-off time is also less than 300 ps. The 20–40 GHz switch has lower resistance in the bias network than the dc–40 GHz switch, and thus switches somewhat faster.

VI. Switch Device Figure of Merit

Switch device figure of merit (quality factor) may be expressed in terms of the switch FET equivalent circuit in Fig. 1(c). Cut-off frequency figures of merit are also used, and may be derived from quality factors. The simple switching quality factor (Q_s) is defined as the ratio of the "off" state device impedance to the "on" state device impedance. For the equivalent circuit in Fig. 1(c) this yields the following relationship:

$$Q_s = \frac{\left[(R_{off})^2 + (1/\omega C_{off})^2\right]^{1/2}}{R_{on}}$$

but since $(1/\omega C_{off}) \gg R_{off}$, the relationship can be simplified to

$$Q_s \approx \frac{1}{\omega R_{on} C_{off}}.$$

This relationship does not include R_{off}, and thus is an inaccurate figure of merit for broad-band switching. A simple empirical modification can be made to include the

effect of R_{off}:

$$Q_s' = \frac{1}{\omega R_{on} R_{off} C_{off}}.$$

Q_s and Q_s' may be calculated for the devices used in the dc–40 GHz and 20–40 GHz switches from the equivalent circuit values that have been determined. Q_s for these devices ranges from 4.4 to 4.9 at 40 GHz, while Q_s' is 6.3 to 7.0 at 40 GHz.

The other figure of merit commonly used for switching devices is the Kurokawa and Schlosser quality factor ($\hat{Q}$). For the FET model in Fig. 1(c), $\hat{Q}$ is expressed as follows:

$$\hat{Q} = \left[\frac{(R_{on} - R_{off})^2 + (1/\omega C_{off})^2}{R_{on} R_{off}} \right]^{1/2}.$$

With this relationship $\hat{Q}$ is calculated to be from 9.3 to 9.75 for the devices in the dc–40 GHz and 20–40 GHz switches. The relationship above can be further simplified if it is assumed that $(1/\omega C_{off})^2 \gg (R_{on} - R_{off})^2$, yielding

$$\hat{Q} \approx \frac{1}{\omega C_{off} \sqrt{R_{on} R_{off}}}.$$

Note that this is similar to the relationship for Q_s', but has a weaker dependence on R_{on} and R_{off} (and thus is more dependent on C_{off}). Since the switches presented in this paper incorporate C_{off} into an artificial transmission line, the strong dependence of $\hat{Q}$ on C_{off} is excessive. Of the three figures of merit, Q_s' most closely predicts the relative performance of devices in the broad-band switches described in this paper. However, $\hat{Q}$ is the better general-purpose quality factor. None of these figures of merit is completely accurate in predicting relative switch performance for different devices. With any of these figures of merit, very different performance can be achieved from two devices having the same value of Q. Only a model for actual switch performance can completely predict the performance of a switch circuit with any given switch device.

VII. Summary

Two millimeter-wave switches have been demonstrated: one covering 20 to 40 GHz, the other dc to 40 GHz. Conventional millimeter-wave FET's were used to allow the switches to be easily integrated with existing millimeter-wave amplifiers. Although these are not extraordinary switch devices, adequate switch performance has been achieved. Performance can be adequately modeled with the simple switch FET model in Fig. 1(c). The equivalent circuit element values have been determined. R_{on} is 2.7 to 3.0 $\Omega \cdot$mm, C_{off} is 0.3 pf/mm, and R_{off} is 0.7 $\Omega \cdot$mm. It has been shown that all of these elements are important to the performance of broad-band switches. In particular, R_{off} is a significant contributor to insertion loss, as the switches reported in this paper demonstrate.

Expressions for switching quality factor (Q) for the switch FET equivalent circuit in Fig. 1(c) have been derived. Neither of the commonly used switch figures of merit adequately predicts the performance of devices in the circuits presented in this paper. A variation on simple switch quality factor (Q_s') more accurately predicts switch device performance for these circuits. However, the use of any switch device figure of merit can be misleading. Only modeled circuit performance can accurately predict the performance of a switch with a given device. It has been shown that a relatively simple model can have adequate accuracy to 40 GHz.

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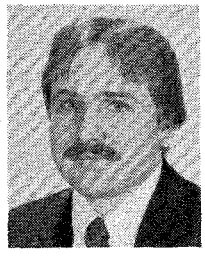

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